KamLAND data format provided by the front end electronics

Version 2.0

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Thorsten Stezelberger

1 Introduction

The waveform data of KamLAND has to be stored in a convenient way. This paper shows the preferred format for the front end (FE) design. The format is based on the proposed format of Enomoto Sanshiro from 12 Nov. 1999.

2 Data format

The following picture gives an overview about the planned data format and the location of the data within the data block.

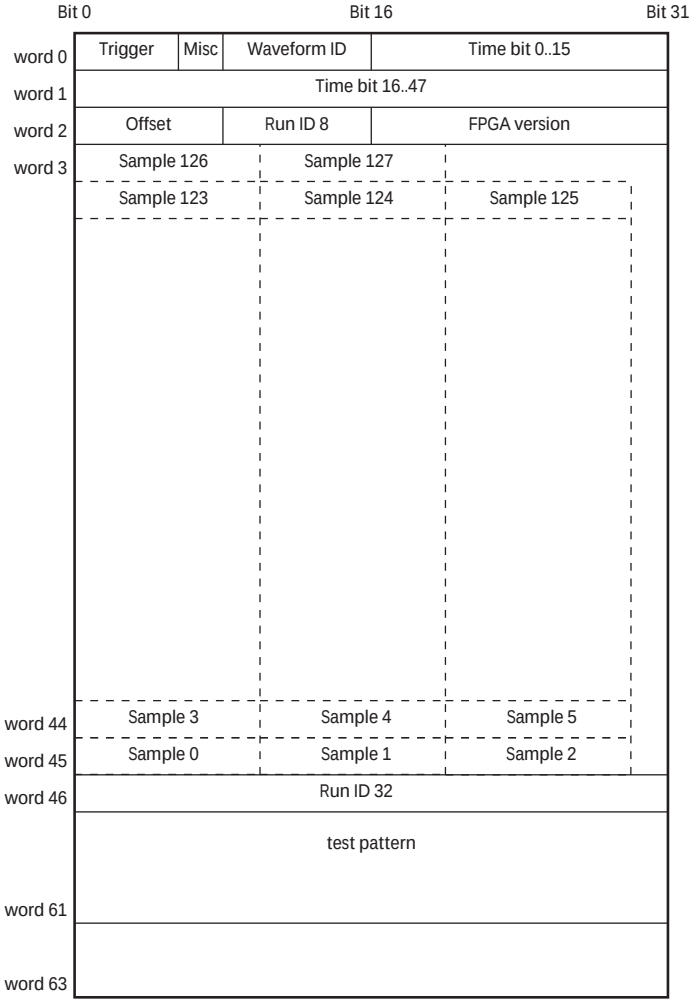

Figure 1: Data format

The following tables show the data format more detailed.

Bit 0..4	Trigger information provided by the trigger system
Bit 5	ATWD launch right after “retrigger” time
Bit 6	ATWD launch right after both ATWD were busy
Bit 7	Discriminator fired during ATWD acquisition
Bit 8..14	Waveform ID (for details see below)
Bit 15	Reserved for future use
Bit 16..23	Trigger time stamp bit 0..7
Bit 24..31	Trigger time stamp bit 8..15

Table 1: Word 0

Bit 8	ATWD A/B (ping/pong)
Bit 9..12	PMT channel on the FE board
Bit 13..14	Gain channel

Table 2: Format of the Waveform ID

Value	Gain
0	High (x20)
1	Medium (x4)
2	Low (x0.5)
3	40MHz system clock

Table 3: Gain channels of the ATWD

Bit 0..7	Trigger time stamp bit 16..23
Bit 8..15	Trigger time stamp bit 24..31
Bit 16..23	Trigger time stamp bit 32..39
Bit 24..31	Trigger time stamp bit 40..47

Table 4: Word 1

Bit 0..7	Offset between Trigger time stamp and ATWD launch
Bit 8..15	Run ID 8
Bit 16..31	Version number of the channel FPGA code

Table 5: Word 2

The next table shows the location of the samples within a 32 bit word. The order of the samples (see figure 1) is due to the design of the digitizer chip (ATWD). A change of the order would increase the FPGA design at the FE and a potential error source.

For the LWords 4 till 45 there are 3 Samples within 1 LWord (see table 6). The first LWord with waveform information (LWord 4) has only two samples (samples 126 and 127).

Bit 0..9	Samples 0
Bit 10..19	Samples 1
Bit 20..29	Samples 2

Table 6: Location of samples within a LWord

The LWords 46 to 61 contain a test pattern to make it easier to find front end electronics board problems. This test pattern allows it to find and identify dropped data bits. Table 7 shows the test pattern.

LWord	Pattern (hex)
47	ffffffff
48	00000000
49	55555555
50	aaaaaaaa
51	ffffffff
52	00000000
53	55555555
54	aaaaaaaa
55	ffffffff
56	00000000
57	55555555
58	aaaaaaaa
59	ffffffff
60	00000000
61	55555555

Table 7: Test pattern at the end of the data

Undefined bit are not used and can be used in future or for debug reasons. One should not assume that these bits are always 0 or 1.

3 Revision history

12/11/2000 Changed to 3 samples per LWord.
12/20/2000 Changed to 3 sample data format.
01/12/2001 Change of 3 sample data format (request Enomoto Sanshiro).
01/17/2001 Change of figure 1.
01/04/2002 Test pattern added to waveform; Channel FPGA version added to header; Added Run ID 8 bit
03/06/2002 Added Run ID 32 bit
03/12/2002 Added status bit for launch after retrigger time or both ATWD busy
09/09/2002 Added bit “Discriminator fired during ATWD acquisition”